X-band sampling technology demonstration

Stephane Halté, Cédric Chambon, Stephen Rawson, Abhijeet Dasgupta, Guillaume Neveux, Denis Barataud

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Denis Barataud, Halte Stephane, Cédric Chambon, Rawson Steven, Abhijeet
Dasgupta, Guillaume Neveux, Halté Stéphane, Stephane Halte@esa, Dasgupta
Int, Chambon Cédric, et al.

X-Band Sampling Technology Demonstration

Halté Stéphane
ESOC
Darmstadt, Germany
Stephane.Halte@esa.int

Chambon Cédric
CALLISTO France SAS
Villefranche de Lauragais, France
Cedric.Chambon@callisto-space.com

Rawson Stephen
CALLISTO France SAS
Villefranche de Lauragais, France
Steve.Rawson@callisto-space.com

Dasgupta Abhijeet
XLIM UMR CNRS-7252
Limoges, France
Abhijeet.Dasgupta@unilim.fr

Neveux Guillaume
XLIM UMR CNRS-7252
Limoges, France
Guillaume.Neveux@unilim.fr

Barataud Denis
XLIM UMR CNRS-7252
Limoges, France
Denis.Barataud@unilim.fr

Abstract— **The technical objectives of this project are to simplify the Ground Station architecture currently used by European Space Agency in Deep Space Antenna by implementing the concept of Software Defined Radio. This paper summarizes the experimental results obtained at the preliminary and detailed design phases. The reception RF signals have been sampled using commercially available Track and Hold amplifier and digitized using Analogue-to-Digital Converter. The transmission RF signal have been synthetized using high-frequency Digital to Analogue Converters.**

Keywords—Ground station, RF sampling, digitization, digital signal processing

I. INTRODUCTION

The European Space Agency (ESA) tracking station network (ESTRACK) is at present composed of three 35m antennas for Deep Space (DS) missions and several smaller antennas in the range 15m - 6m for Launch and Early Orbit Phase (LEOP) services and Earth Observation (EO) missions. The primary communications functions fulfilled by each ESTRACK station are collectively referred to Tracking Telemetry & Command (TT&C). The frequency plan used for the Near Earth (NE) and DS communications services are allocated in S-, X-, K- and Ka-bands and are shown in Table I. In addition, a simplified block diagram of the ESA Ground Station architecture for multiband signal reception is shown in Fig. 1. The current configuration has different antenna feed systems for each of the received frequency bands. Typically, the feeds which use band limited corrugated feed horns with Ortho Mode Transducer (OMT) and produce Radio Frequency (RF) outputs in dual orthogonal polarisations which are connected to RF Low Noise Amplifiers, then down-converted to Intermediate Frequency (IF) at L-band before being digitised and demodulated using Software-Defined radio (SDR) techniques by the Tracking Telemetry & Command Processor (TTCP). The down-converters currently employed are analogue technology containing RF and IF filters, mixers, and local oscillators and are specifically designed and produced for each designated frequency band.

For over two decades [1], the SDR technology has promised to revolutionise the communication industry by delivering low-cost and flexible software solutions for communication protocols. In the last ten years, the development of Field-Programmable Gate Array (FPGA), programmable RF transceiver system-on-chip and multi-GSps Analogue-to-Digital Converter (ADC) or Digital-to-Analogue Converter (DAC) can fulfil the early promise and introduce the concept of SDR. Many concepts and developments can be found in the scientific literature. Among the most relevant for the present studies, [2] deals with space communication systems based on Components-Off-The-Shelf (COTS), [3]

presents the main blocks of a SDR-based architecture and [4] paves the way for engineers to better understand and implement SDR concepts in RF communication systems. As a result, the main attributes to implement SDR in a RF communication system are to minimize the number of RF hardware components like mixers, oscillators or filters because replaced by digital functions, minimize maintenance and procurement costs compared to a traditional architecture, counteract analogue RF chain imperfections (interference, distortion, aging) with easily-reprogrammable digital functions, increase flexibility to support multiple signals from multiple spacecrafts and increase configurability/re-configurability by simplifying new software function installation.

The aim of the study is to develop S- and X-bands breadboard containing a sampler architecture to down convert the incoming RF signal to IF and digitise it with adequate ADC. Doing this will prove the concept of sampling RF signal directly at S- and X-bands without the traditional down conversion of the RF signal.

TABLE I.   ESA GROUND STATION FREQUENCY BANDS.

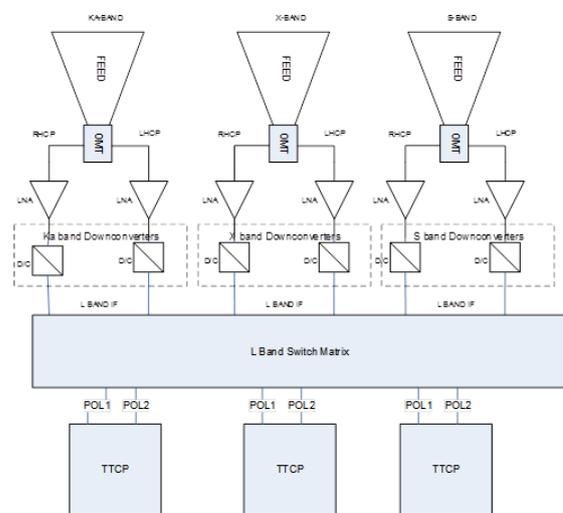| RF bands	Service	Downlink frequency	Uplink frequency
S	DS	2.29-2.3GHz	2.11-2.12GHz
	NE	2.2-2.29GHz	2.025-2.11GHz
X	DS	8.4-8.45GHz	7.145-7.19GHz
	NE	8.025-8.4GHz 8.45-8.5GHz	7.19-7.235GHz
K	NE	25.5-27GHz	N/A
Ka	DS	31.8-32.3GHz	27.5-31GHz 34.2-34.7GHz

Fig. 1. Multiband reception architecture used by ESA ground stations

The first objective is to output the IF signal within the TTCP input bandwidths (RF sampler mode). The second objective is to digitise directly the incoming RF signal with a high-speed ADC (RF digitiser mode). Finally, the last objective is to compare both quality of signals to demonstrate the RF direct sampling concept.

II. RF SAMPLING CONCEPTS

To achieve the objectives of SDR, the RF incoming signal shall be converted in the digital domain using RF Sampling and digitization stages. The digital signal is then processed to produce baseband I/Q outputs. The Nyquist–Shannon sampling theorem applies to low-pass sampling, like baseband signals centered around 0Hz. Following this theorem, the maximum frequency F_{RF} of the RF signal is limited and shall not exceed half the sampling frequency F_S. On the other side, the theory of band pass sampling [5] applies to RF signals occupying a certain bandwidth $B = F_H - F_L$, with F_H the high frequency and F_L the low frequency. In the frequency domain, the digitizer (or a sample & hold stage) generates harmonics at integer multiples of the sample frequency and replicates the spectrum. The aim is thus to calculate F_S where no aliasing occurs by considering the following inequation:

$$\frac{2F_H}{n} \le F_s \le \frac{2F_L}{n-1} \qquad (1)$$

The replication order n is an integer between 1 and the greatest integer less than or equal to F_H/B. This concept is illustrated at Fig. 2 where the first spectrum replication (order $n-1$) is obtained between $F_S/2 - F_S$, then the second spectrum replication (order n) is obtained over $0 - F_S/2$, which corresponds to the first Nyquist Zone (NZ) of an ADC. To avoid spectrum overlapping, it can be clearly seen that half the sample rate shall be chosen greater than F_H/n and lower than $F_L/(n-1)$. It is possible to compute the necessary spectrum replication order n to fulfill the down-conversion of the RF bands listed in Table I. Unfortunately, even if the integer n could match today's available sample rates, it is not possible to select a commercial ADC with an analogue input bandwidth as broad as 32GHz while considering resolution in the order of 10 bits.
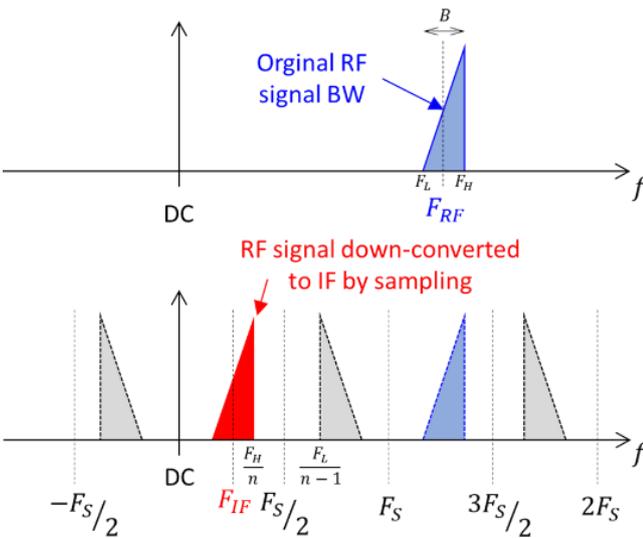

Fig. 2. Illustration of frequency down conversion using bandpass sampling concept

The concept of RF aliasing can be used in the receiver to subsample an RF signal well beyond the ADC sample rate and thus enlarge the analogue input bandwidth of a digitizer [6]. The Track and Hold Amplifier (THA) technology is a critical component used as a sampler and thus able to convert RF bands into relatively low IF bands in accordance to the following relation:

$$RF = \pm IF + nF_s \qquad (2)$$

In the same way, the concept of RF spectrum aliasing can be used to transmit RF signals. The commercially-available RF DAC reference EV12DS460 from E2V is capable of aliasing large synthetic bandwidth into higher NZ whilst maintaining good spectral purity. As an example, the Fig. 3 shows the seven aliased images of a 1GHz test signal across the first eight Nyquist zones at the output of the DAC sampling at a rate of 6GSps. The digital IF signal at 1GHz is visible in NZ1 but several aliased images are generated at F_{out} and also appear in all the following NZs following the relation:

$$F_{out} = \pm IF + nF_s \qquad (3)$$

Four different output pulse shaping modes have been considered: Non-Return to Zero (NRZ), Return To Zero (RTZ), Narrow Return To Zero (NRTZ) and RF. As it can be seen, selecting a specific pulse shaping mode optimizes the DAC dynamic response to a given output RF band. Applying bandpass filtering and power amplifying to the RF signal at the DAC output provides a synthetic analogue image in the RF domain of a transmit signal without using analogue components like mixers and local oscillators.

III. RF SAMPLING ARCHITECTURES

A. RF sampler mode

The RF sampling configuration consists in sampling the RF incoming signal to get out IF signal within TTCP bandwidth.

Fig. 3. RF signal aliasing effects with E2V EV12DS460 DAC sampling at 6GSps

TABLE II. SUMMARY OF CALCULATED THA SAMPLE RATE FOR RF SAMPLER MODE.

Service	THA sample rate	n	IF to TTCP
S-band NE	2780MSps	1	535±45MHz
S-band DS	2780MSps	1	485±5MHz
X-band NE1	3746MSps	2	720±188MHz
X-band DS	3960MSps	2	505±25MHz
X-band NE2	3960MSps	2	555±25MHz
K-band NE1	3900MSps	7	1550±250MHz
K-band NE2	3971MSps	7	1550±250MHz
K-band NE3	3600MSps	7	1550±250MHz
Ka-band DS	3813MSps	8	1550±250MHz

The RF sampler breadboard block diagram is shown at Fig. 4. Several key analogue functions are implemented to condition the incoming RF signal before the THA. First of all, LNAs are used to increase the incoming signal power level, without degrading the Signal-to-Noise Ratio (SNR) and a controllable attenuator is used to decrease the incoming signal power level to avoid following RF components to saturate. An electro-mechanical switch is used to steer the common sampler input port to the S- and X-bands input ports. DC blocks and 180° hybrid couplers are used to optimise the RF performance of the THA. The clock signal is generated with an ultra-low phase noise Phase-Locked Loop (PLL)-based circuit that allows frequency generation up to 19GHz with phase noise Root Mean Square (RMS) jitter as low as 50fs with the adequate 10MHz frequency reference.

The THA reference RTH090 form Teledyne Scientific and Imaging has been selected for the project, thanks to its very broad input analogue bandwidth which specified up to 25GHz. In addition, the sample rate is specified at 4GSps but has been tested up to 8GSps. This device can sample S- and X-bands and Ka-bands signals as well. The THA nonlinear model has been extracted, simulated using harmonic balance algorithm and successfully compared to results in the datasheet [7]. In addition, the frequency plan and THA sample rates have been calculated, confirmed with MATLAB simulations and is shown at Table II. The THA sample rate shall be selected as high as possible to limit the spectrum replication, the additive noise aliasing and the phase noise jitter.

On the other hand, the sample rate shall be as low as possible to optimise the clock phase noise. From these two antagonistic phenomena, the THA sample rate selection is the result of a trade-off between the ability to generate high-frequency low-phase noise signals (with extremely low RMS jitter) and still meeting the noise figure (additive noise) performance.

B. RF digitiser mode

The commercial ADC reference selected for the project is the reference ADQ7DC from SP Devices. The RF sampling and digitisation configuration consists in sampling the RF incoming signal to get an IF signal within the first NZ of the ADC which is over 0 - 2.5GHz, but best performance is obtained up to 1GHz. The ADC sample rate is selected at 10GSps with only one operating channel or 5GSps for dual-channel operation. The IF frequency is minimized in order to avoid conversion loss due to the cardinal sine frequency response of the THA. The Table III summarises all the lowest IF frequencies and the THA sampling rates. The RF sampler and digitiser breadboard block diagram is shown at Fig. 5. The analogue front-end consists in the previous RF sampler breadboard connected to the ADQ7DC ADC with an adequate antialiasing band pass filter in between. The ADC comes with its own clock frequency generator and a common 10MHz reference can be used to synchronise the RF sampler and the ADC.
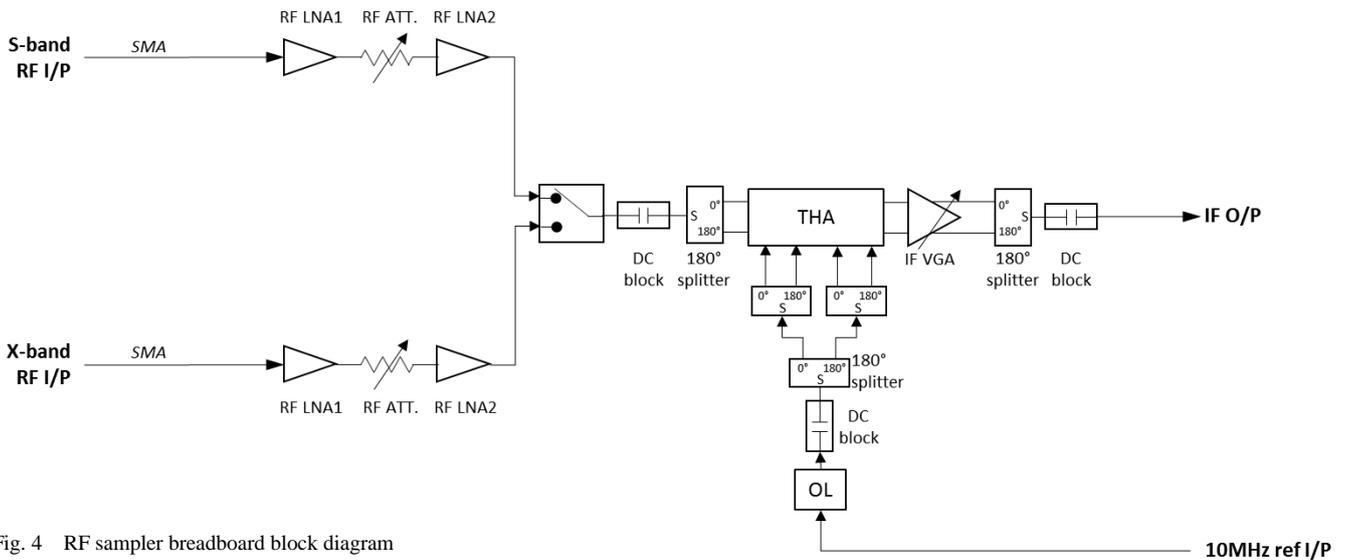

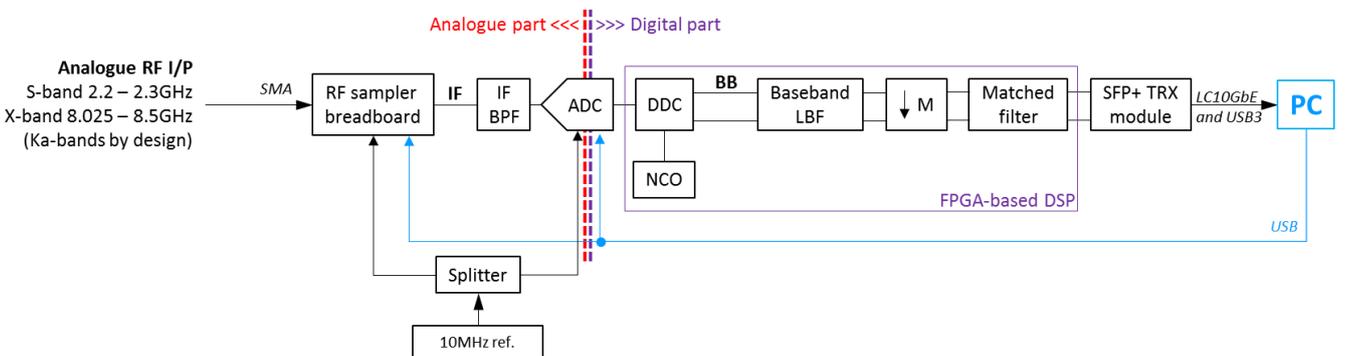Fig. 4   RF sampler breadboard block diagram

Fig. 5   RF sampler and digitiser breadboard block diagram

Service	THA sample rate	n	IF to TTCP
S-band NE	2400MSps	1	155±45MHz
S-band DS	2400MSps	1	105±5MHz
X-band NE1	3950MSps	2	313±188MHz
X-band DS	3950MSps	2	525±25MHz
X-band NE2	3950MSps	2	575±25MHz
K-band NE1	3728MSps	7	350±250MHz
K-band NE2	3800MSps	7	350±250MHz
K-band NE3	3871MSps	7	350±250MHz
Ka-band DS	3962MSps	8	350±250MHz

The digital back-end is mainly operated with ADC onboard FPGA which acts a Digital Signal Processing (DSP) unit. The main DSP functions are firstly a digital downconversion stage to near DC with a Numerically-Controlled Oscillator (NCO) running at a programmed frequency which is the IF carrier frequency. The output is complex I/Q samples at the ADC sampling rate. Secondly, a decimation low pass filter followed by programmable decimation are used to reduce sample rate. The third DSP function is a matched filter is used to optimise SNR when receiving extremely low signal power. Finally, a Small Form-factor Pluggable (SFP+) transceiver module with Lucent connector (LC) is used to drive optical fibre channel. The decimated complex I/Q samples are transmitted using a 10GbE interface.

IV. EXPERIMENTAL RESULTS

A. THA commercial device

The RTH090 THA is a very critical components and an evaluation module has been purchased after the preliminary design phase to measure and validate the RF performance. The first parameter to be measured and compared to the datasheet is the conversion loss. An input signal of -6.5dBm or 0.3Vpp has been generated and the output signal has been measured at IF. Fig. 6 shows the conversion losses measured up to 32GHz and considering sample rates of 2 and 4GSps. It can be seen that the 3dB bandwidth is around 28GHz for both configuration and is significantly degraded (by 7dB) at 32GHz. The conversion has been measured at various input power levels to get the compression points. The Fig. 7 shows the results measured at 2.3, 8, 26.25 and 32.05GHz at various sample rates. The output 1dB compression points have been measured around -3dBm at S- and X-bands, around -6dBm at K-band and around -10dBm at Ka-band.

The Noise Figure F (NF) of the THA has been also calculated from the phase noise floor measurements $S_{\Phi floor}$ according to the following relation [8]:

$$S_{\Phi\,floor} = \frac{FkT_0}{P_{in}} \qquad (4)$$

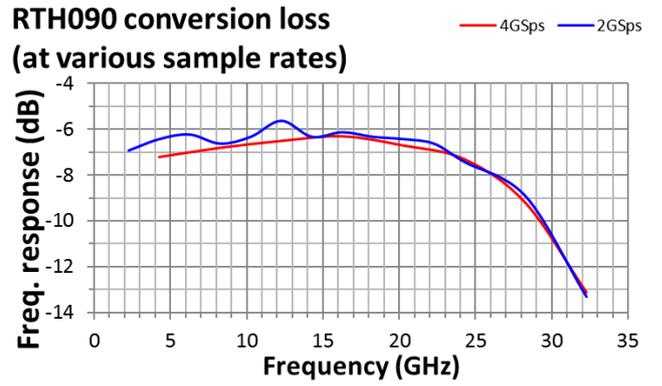Where k is the Boltzmann Constant, T_0 is the room temperature and P_{in} is the input RF power level.

Fig. 6 RTH090 measured conversion losses up to 32GHz

The Fig.8 shows measured NF for X- and K-bands RF input signal, at various input power levels and considering various sample rates. It can be seen that the NF is firstly degraded at high input power, because the nonlinear effects increase the noise spectrum aliasing. Secondly, the NF is optimized at higher sample rate, because in this case the spectrum replication order n is limited and the noise spectrum aliasing is lowered. The maximum NF have been measured for all the RF ranges of interest and summarized in Table IV.

B. THA + ADC commercial device

Some preliminary tests have been performed with the RTH090 THA used as a RF sampler to convert RF signals down to a common IF at 0.1GHz , filtered with an anti-aliasing band pass filter and then digitised using ADQ7DC ADC at a sample rate of 10GSps and considering a Full Scale (FS) of 1Vpp (which corresponds to +4dBm with 50Ω impedance line) .

TABLE IV. SUMMARY OF THA MEASURED NF.

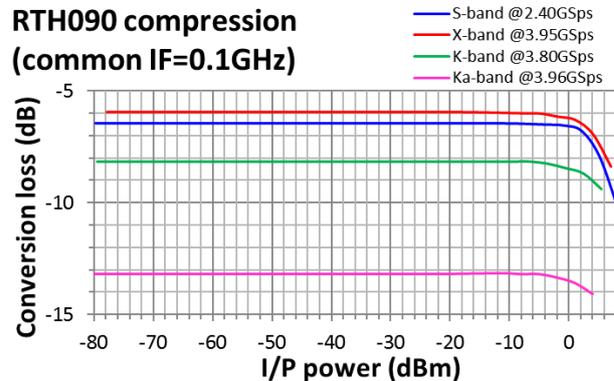| RF	Sample rate	NF
2.3GHz	2.40GSps	28.5dB max
	1.20GSps	31.5dB max
8.0GHz	7.90GSps	25.0dB max
	3.95GSps	27.0dB max
26.25GHz	3.65GSps	29.0dB max
	3.80GSps	29.5dB max
32.05GHz	7.93GSps	33.0dB max
	3.96GSps	34.0dB max

Fig. 7 RTH090 measured compression points at S-, X-, K- and Ka-bands

Fig. 8   RTH090 measured noise figures at X- and K-bands

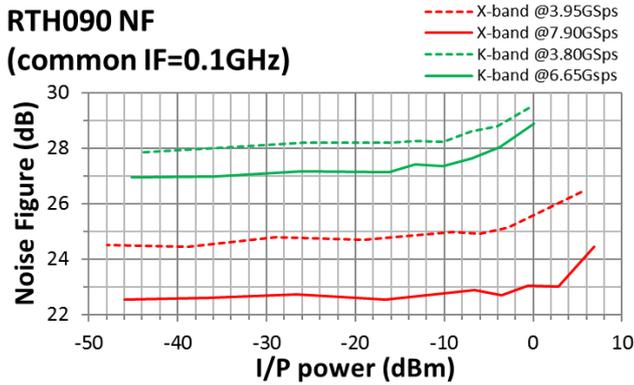Fig. 9   RTH090 measured noise figures at X- and K-bands

Fig.10   RTH090 measured noise figures atX- and K-bands

The signal is displayed in time- and frequency domains using SP Devices graphical user interface (ADCaptureLab). In addition, the signal is processed to measure two key-parameters: the SNR and the Spurious-Free Dynamic Range (SFDR). The Fig. 9 shows the measured SFDR which is optimal (greater than 70dBc) over a very broad range of input signal power level (-25 to -5dBFS). A significant drop of SFDR performance can be seen around -1dBFS which is due to the ADC input protection circuit. At lower input power level, the SFDR is limited by noise. The Fig. 10 shows the measured SNR, within the same conditions. Here again, a significant clipping phenomenon is visible around -1dBFS. But the SNR remain greater than 30dB for the same input power level of -25 to -5dBFS.

The SFDR and the SNR are always measured at 0.1GHz IF and the performance is very similar for all the sampled RF ranges from S- to Ka-band. That proves the feasibility to sample and digitise with a high-level of performance the ESA DS and NE RF signals.

V.   Conclusion

This paper presents the major results obtained for the RF sampling technology demonstration project for ESA. The sampling and digitisation of RF signals used by ESA's ground stations have been successfully proven using commercial electronic devices like the RTH090 THA and the ADQ7DC ADC. The THA is able to operate up to 32GHz at a sample rate of 8GSps and the ADC operational bandwidth has been validated up to 2.5GHz. Some preliminary results have been obtained with the RF sampler and digitiser configuration (ADC + THA). Considering input power level over -25 to -5dBFS, the SFDR has been measured greater than 70dBc and SNR greater than 30dB. The next step is to develop and build a RF sampler demonstrator that will be tested in the Callisto laboratory and also in ESA ground station.

Regarding the transmission aspects, it was possible to synthetize S- and X-bands signal with very good phase noise and SFDR performance. The results measured at Ka-bands are out of ESA specification for the application, but recent release of other RF DAC commercial references with higher sample rate shrinks the technological gaps to generate high-quality analogue signals around 30GHz.
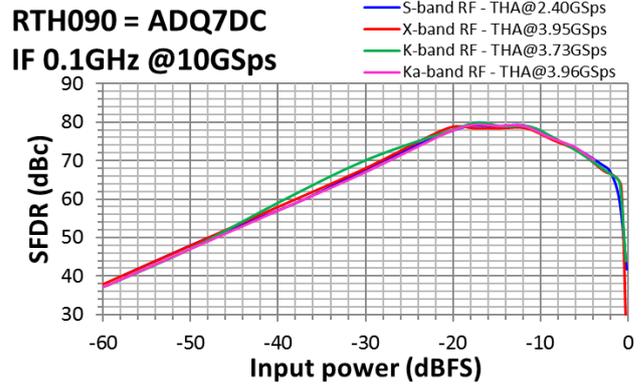
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