An Envelope Tracking oriented, 17-20GHz, Average 64QAM Modulated 2W, PAE>37%, OBO 8dB GaN MMIC Power Amplifier

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***Abstract*— This article presents the design and the realization of a 4W reactively-matched Power Amplifier (PA), in GaN MMIC technology operating in the 17-20 GHz band. The design has been oriented to be used with Envelope Tracking (ET) systems. The designed PA for Envelope Tracking (PA-ET) is a two-stage reactively-matched PA and it is based on the use of three power transistors from the UMS GaN GH15 technology. Large signal characterizations with 64 QAM modulation show that PA-ET provides an average dynamic output power ($\bar{P}_{outdyn}$) greater than 2 W (33 dBm) associated to an average dynamic Power Added Efficiency ($\overline{PAE_{dyn}}$) greater than 37 % and an insertion gain (G_{Idyn}) greater than 11 dB in the 17-20 GHz band. The ET improves efficiency performance by 21 points compared to a PA using the same technology with fixed bias.**

Keywords*— *High power amplifiers, envelope tracking, linearity

I. Introduction

In the context of modern radiocommunication systems that cover millimetric frequencies, the data rates are constantly increasing, implying thus greater electrical consumption. The fundamental thermal management at PA level is there more complex. The PA efficiency must be improved over wide bands at RF frequencies. In addition, the modulated signals used have high Peak to Average Power Ratios ((PAPR)): around 10dB for an LTE signal. PAs must therefore present a significant PAE associated with a good linearity along a large Output Power Back Off (OBO) The efficiency of a conventional amplifier must therefore be greatly improved along a large OBO. The average added power efficiency of an amplifier stage is expressed as a function of the average drain efficiency and the average power gain according to the following equation:

$$\overline{PAE_{dyn}}[\%] = \bar{P}_{outdyn}(t)/\bar{P}_{DC}(t) \times \left(1 - \frac{1}{\overline{G_{Pdyn}}}\right) \text{ with } \overline{G_{Pdyn}} = \frac{\bar{P}_{outdyn}(t)}{\bar{P}_{indyn}(t)} \quad (1)$$

The optimization of the average $\overline{PAE}$ is carried out on the one hand by the choice of the quiescent operating point, on the other hand by the search for the maximum average drain efficiency. This optimization can be done by minimizing the DC drain current and/or voltage on the OBO.

The ET technique seems to be one of the architectures to achieve the best trade-off between efficiency, linearity and bandwidth for systems with high PAPR signals as the ones required in the next future generations of radiocommunications (5G and beyond) [1]. The envelope tracking technique allows the achievement of the optimization of $\overline{PAE_{dyn}}$ thanks to the direct application of a shaping envelope control law on the drain bias of the PA. The choice of this shaping envelope control law offers the inherent capability of this technique to improve the linearity in terms of AM/AM conversion [2]. Finally, the ET technique enables a management of the efficiency/linearity trade-off with a high flexibility. The paper first introduces GaN HEMT 0.15 µm technology. The design method is detailed in paragraph III. The results of experimental microwave time-domain characterizations of the PA-ET driven by modulated signals with a drain shaping envelope control law for linear constant average power gain are finally presented.

II. GaN HEMT 0.15 Micrometres Technology

The PA-ET is based on the use of AlGaN/GaN HEMTs with 0.15 µm gate length (called GH15 technology) from the UMS foundry. The GH15 technology is qualified on a 4" diameter SiC substrate for a 25 V drain-source extrinsic bias voltage. The breakdown gate-drain voltage is greater than 90 V and the pinch voltage which characterizes the Schottky contact is around -3.2 V. For optimal matching, the GH15 transistor provides a saturated microwave output power of 3.5 W/mm associated with a maximum PAE around 45% at 30 GHz [3].

III. Design of the PA-ET

The principle of PA-ET is detailed in Fig. 1.

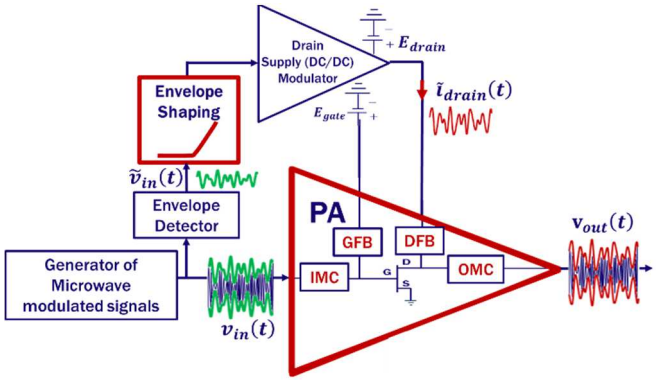


Fig. 1. Operating principle of PA-ETs.

The red highlighted functions of Fig. 1 have been implemented. They consist in the design of a K-band PA-ET and the drain voltage shaping envelope control law applied ($v_{DS}(t)$) to the realized PA-ET. The topology associated with the most efficient PA-ET design method is depicted in Fig. 2.

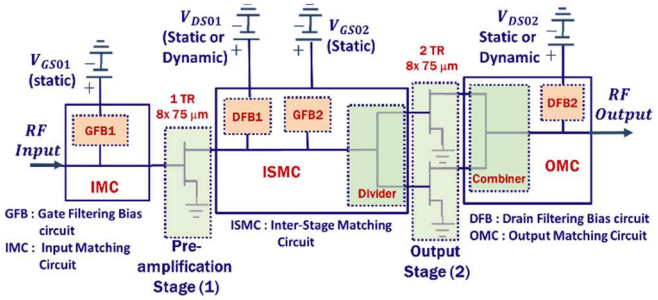


Fig. 2. 2-stage reactively-matched PA-ET topology.

A 2-stage reactively-matched PA-ET architecture (1 power stage and 1 pre-amplification stage) was chosen to ensure sufficient power and gain performances. In the following and for sake of simplicity, the matching circuits will be called "2-port" matching circuits, even if, in fact, they are 3-port or 4-port matching circuits since there is, at least, one input associated to the power supply and associated to a combiner sometimes. The design method consists firstly in determining the Output Matching Circuit (OMC). This second stage OMC contains the Drain Filtering Bias 2-port (DFB2) and the combiner of the two GH15 8x75 µm transistors of the output stage. To design the OMC, optimal load admittances and optimal source impedances are determined for variable drain voltages (Sweep of V_{DS0} between 5 V and 22 V) at the fundamental and 2nd harmonic frequencies (simulated and measured source-pull and load-pull).

Fig. 3 shows the simulated load-pull results giving the optimal load admittances for a single GH15 8x75 µm transistor at 17 GHz, 18.5 GHz and 20 GHz (with a pre-matching of the reactive part of the transistor input and for load and source harmonic impedances equal to 50 ohms). Fig. 3 shows an example of the three optimal area to obtain, for a chosen 13 dB OBO and a CW $\bar{P}_{out}(f_0)/\hat{P}_{out}(f_0)$ ratio higher than 90 %:

- CW PAE higher than 45 % at 17 GHz and 18.5 GHz
- CW PAE higher than 40 % at 20 GHz

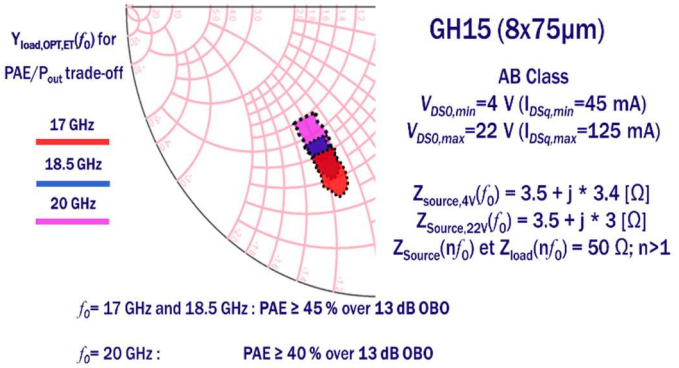


Fig. 3. Optimal load admittance areas for CW $\overline{PAE}$, $CW\bar{P}_{out}(f_0)$ trade-off at V_{DS0}=4 V and V_{DS0}=22 V for 3 frequencies.

Once this characterization of the transistor has been carried out, it is possible to begin the various design steps of the matching circuits of the 2-stage reactively-matched PA-ET.

Finally, the last step consists in designing the Input Matching Circuit (IMC) after obtaining the optimal source impedances at the fundamental frequency for different values of V_{DS0}. Once these values have been obtained, the design of the IMC can be carried out.

Fig. 4 shows the realised PA-ET MMIC chip alone (Left) and the same chip in a test-fixture (Right).

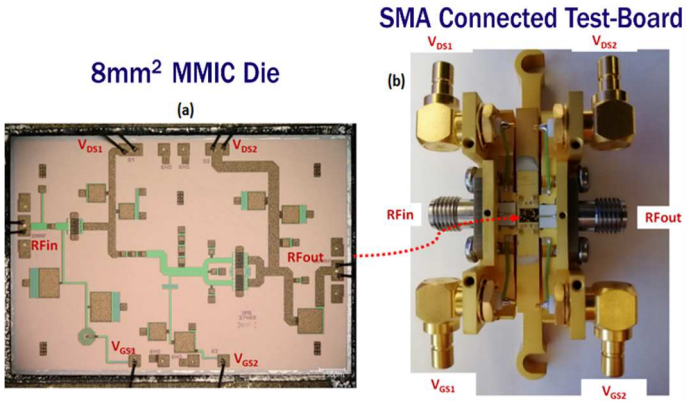
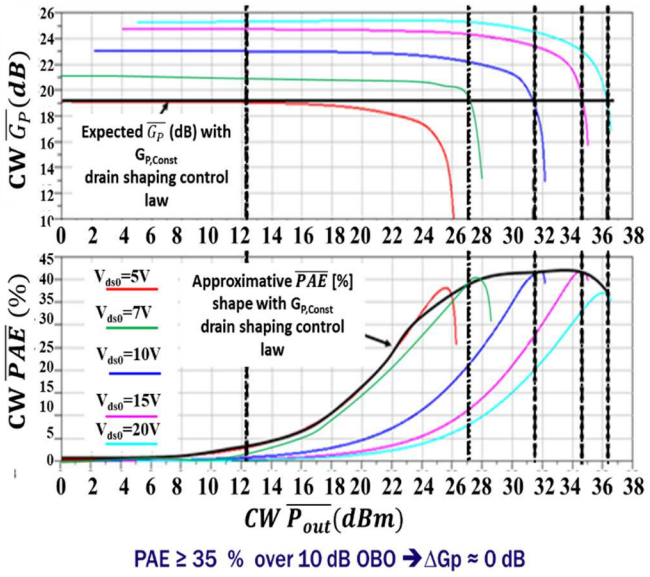


Fig. 4. Realised PA-ET MMIC chip (left) and PA-ET mounted in a test-fixture with SMA connections (Right).

Fig. 5 shows the extraction of a Constant Power Gain (CW $\overline{G_{P,\mathrm{Const}}}(f_0)$) drain shaping envelope control law along the 10dB OBO from the simulated CW power characteristics at 18 GHz for different V_{DS0}.

The application of this drain shaping envelope control law enables maintaining a CW static PAE higher than 35% over 10 dB OBO while cancelling the gain variation. Applying the $\overline{G_P}$,Const drain shaping envelope control law improves the AM/AM linearity of the power gain while maintaining a sufficient PAE performance. This $\overline{G_P}$,Const drain shaping envelope control law (referenced as electromotive force at the direct output of the I/Q modulator V_{emf}) was then applied, in a test-bench for EVM measurement, to the PA-ET driven by modulated signals.



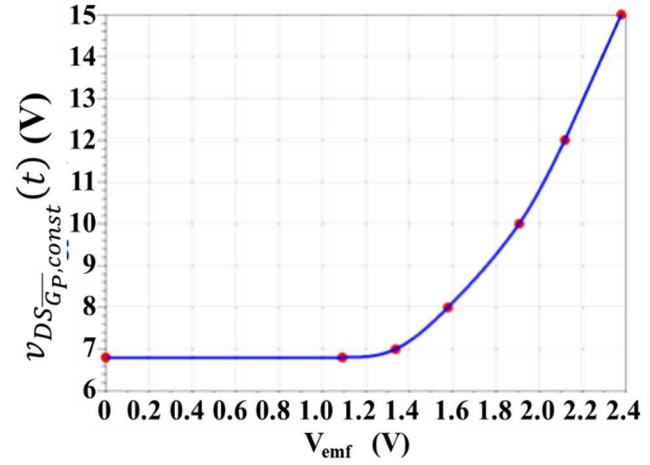


Fig. 5. Extraction (in simulation) of a drain shaping envelope control law ($v_{ds_{\overline{G_P},const}}(t)$) for linear Constant CW $\overline{G_P}$.

IV. PA-ET CW Characterization

Fig. 6 presents a comparison of the measurement and simulation results of the CW $\overline{PAE}$ of the PA-ET carried out under large CW signal operation mode, at 18 GHz for the two drain voltages (minimum and maximum) of the constant power gain drain shaping envelope control law ($\overline{G_P}$,Const). It can be clearly observed that thanks to this constant power gain drain shaping envelope, the AM/AM compensations are already working.

A good agreement is observed between the simulation and the measurement results. The measured PAE is higher than 34 % over 10 dB OBO with a low-level power gain of 17 dB at 5 V and 23 dB at 20 V.

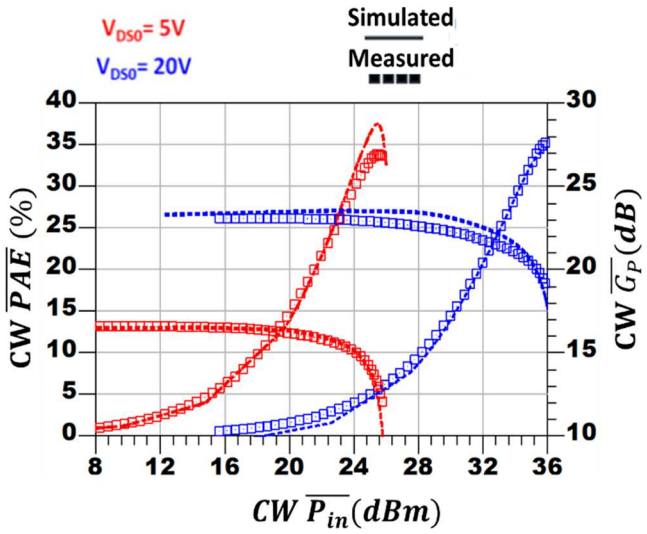


Fig. 6. PA-ET CW measurements at f_0 =18 GHz for V_{DS0} = 5 V and V_{DS0} = 20 V.

V. PA-ET Characterization with a 64QAM Modulation Driven Voltage

The characterizations of the PA-ET (without a fabricated supply modulator) were carried out using a time-domain characterization test-bench, developed at XLIM and based on the generation of modulated RF signals. The test-bench is fully calibrated at RF and LF frequencies. It is shown in Fig. 7.

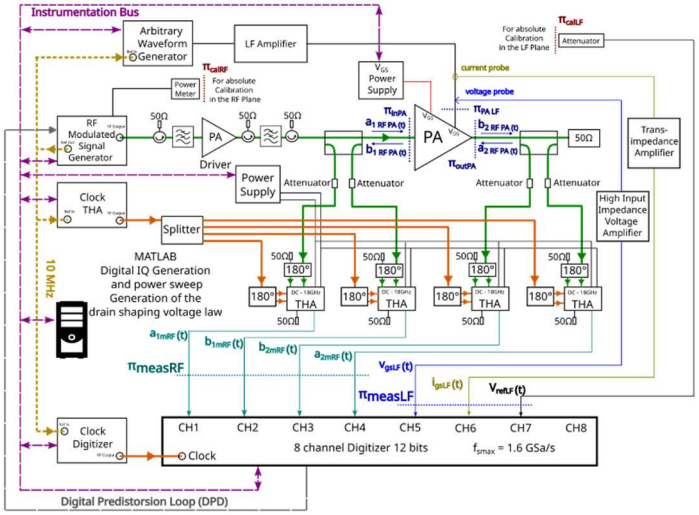


Fig. 7. Block diagram of the time measurement set-up based on the use of an ultra-fast receiver/digitizer (1.6 GS/s) with 8 channels.

Table 1 presents the results of the PA-ET measurements with the $\overline{G_P}$,Const drain shaping envelope control law for a 64QAM modulation, with and without DPD (polynomial without memory) dedicated to AM/PM linearization.

In the 17-20 GHz frequency band, the $\overline{PAE_{dyn}}$ is higher than 35.7 %, the maximum $\bar{P}_{outdyn}(t)$ is higher than 33.8 dBm and the EVM is less than 2.1 % with DPD. At 18 GHz, for the same maximum and average $\bar{P}_{outdyn}(t)$, the DPD reduces the average $\overline{PAE_{dyn}}$ by only 1.1 point but decreases the EVM by 5.1 points.

TABLE I. RESULTS OF PA-ET MEASUREMENTS WITH AND WITHOUT DPD WITH ($\overline{G_{P,\text{CONST}}}$),CONST DRAIN SHAPING ENVELOPE CONTROL LAW

Frequency (GHz)	PA-ET $\overline{G_{P,\text{Const}}}$ Drain law	$\hat{P}_{outdyn}$ (dBm)	$\overline{P}_{outdyn}(t)$ (dBm)	$\overline{PAE_{dyn}}$ (%)	EVM (%)
17	With DPD	34.6	28.7	38	1.4
18	Without DPD	34	27.9	39	7.1
	With DPD	33.8	28	37.9 (-1.1)	2 (-5.1)
19	With DPD	36	29.7	41.2	1.6
20	With DPD	36.6	30	40	2.1

Note that the DPD applied here is for AM/PM linearization only. It has no impact on AM/AM which has already been optimized by the ET method with the $\overline{G_{P,\text{Const}}}$ drain shaping envelope control law.

Fig. 8 presents the dynamic $PAE_{dyn}(t)$ measurement of the PA-ET with a 64QAM input modulation scheme running at 1Msymb/s with a 19 GHz carrier.

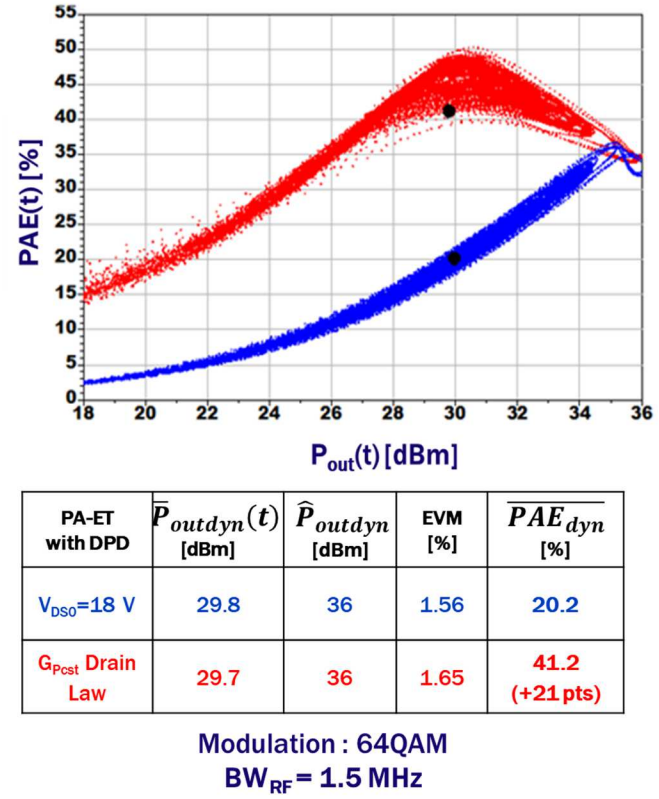


Fig. 8. Time-Domain measurements of PA-ET at f_0 = 19 GHz with AM/PM DPD linearization.

The RF bandwidth is limited to 1.5 MHz due to the use of Maximum 5MHz Low Frequency amplifier in the time measurement set-up shown in Fig. 7. The blue curve corresponds to a static V_{DS0} (18V). The PA-ET is linearized by DPD without memory in both AM/AM and AM/PM. The red curve corresponds to the ET operation of the PA with simple linearization by DPD without memory in AM/PM only. The PAEs are compared for the same $\overline{P}_{out}(t)$ of 29.8 dBm, a maximum $\hat{P}_{out}$ of 36 dBm and with the previous linearizations, the EVM is equal to 1.6%. The PA-ET improves the $\overline{PAE_{dyn}}$ by 21 points which is a higher figure than the result presented in [4] with the power amplifier described in [5].

VI. CONCLUSION

This article presents the design and realization of a two-stage reactively-matched K-band GaN PA-ET demonstrator. The method integrates the ET-oriented simulations of GH15 transistors. The architecture of the PA-ET was chosen in a 2nd stage to respect the specifications. The 3rd step consists in extracting a synchronous V_{DS0} drain shaping envelope control law of the 2 stages, for an ET objective ($\overline{G_{P,\text{Const}}}$ drain) and applying it during the experimental characterization of the PA-ET. A 21 points $\overline{PAE_{dyn}}$ improvement has been measured.

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