Evaluation of a Ku-Band Phased Array's Performances with Co-Simulation Including Measurements

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***Abstract* — A pre-measurement methodology in the design and validation workflow of a full phased array, with radiating elements integrated with commercial-off-the-shelf (COTS) RFIC beamformers, is presented. The process is shown in a 3-step guideline, from the characterization of the beamformer, through the design of the antenna panel, and lastly, to the co-simulation between beamformer characterization data and full-wave simulation results of the radiating array. A clear procedure enables a reliable integration of a full-PCB phased array and a valid comparison to the measurement of the array.**

***Keywords* — phased array, active antennas, RFIC, beamformers.**

I. Introduction

In the past, little interest was shown in the development of phased arrays in the commercial sector due to their excessive costs. Nevertheless, recent research in silicon-based integrated-circuit phased arrays [1] increasingly manifests a pathway to exploit phased arrays as a part of daily-life electronics. The possibility for compact, cost-effective, and mass-produced phased arrays is coming closer to reality than ever. As a result, the development of active phased-array beamforming frontends for ultra-fast communication links in the context of civil 5G and SATCOM communications, with applications in broadcasting, telephone, internet, as well as navigation in far-flung territories, has been concentrated on intensively. Full PCB-based phased arrays utilizing COTS RFIC beamformers have equally been focused on in the last decades due to their low costs, feasibility and scalability. Consequently, numerous developments of PCB arrays have been realized [2][3].

As the integration process of an active beamforming array involves various stages, a thorough design and validation flow is essential. Such clear methodology through the entire integration of the beamforming array facilitates the design process, minimizes errors and eventually, provides a good reference for the measurement of the full array. In this paper, the characterization automatization process, as well as the design of the antenna array and the co-simulation method of the RFIC and the radiating panel are shown. The designers will then be able to anticipate the array performance in the early design phases, and to take corrective actions, such as transitioning modifications in the PCB stackup or excitation weightings corrections to optimize the active antenna gain.

II. Characterization of the RFIC Beamformer

A. Design of a demonstration PCB for the beamformer

The ADAR1000 RFIC Beamformer from Analog Devices, Inc., (ADI), working from 8 GHz to 16 GHz, is selected [4]. The chip includes 4 transmit channels (TX) and 4 receive channels (RX) in single-polarization and half-duplex operation (Fig.1). In both TX and RX operations, the chip provides, reportedly, more than 31 dB gain adjustment range and 360 deg phase adjustment range, with less than 0.5 dB gain variation and 2.8 deg phase resolution. Each RX channel is composed of an LNA at the RX input, followed by a variable-gain amplifier for gain control, and a vector-modulator phase shifter for phase control. A similar configuration is applied for TX channels, where a driver amplifier is connected at the output antenna port.

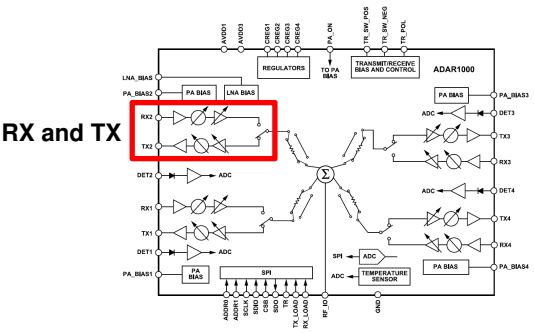


Fig. 1. ADAR1000 RFIC Beamformer.

The wide working frequency bandwidth of the chosen RFIC allows numerous applications of beamforming in 5G and SATCOM in Ku band. Prior to integrating multiple RFICs with the antenna array, it is essential to have a full validation of the functioning of the IC and a comparison with the datasheet from the chip provider. A demonstration PCB is therefore designed to collect S-Parameters (SP) performance of the ADAR1000 RFIC. The proposed board is a modified version of a reference evaluation board from the provider (Fig.2). The chip employs a basic 4-wire SPI with 1.8 V on-chip logic signals, therefore, a pinout for 1.8 V control signals (P1) is connected directly to the chip's pins responsible for the SPI wires. Furthermore, a pinout for 3.3 V logic level (P2) is implemented to offer flexibility since many microcontrollers nowadays use such logic level. A control module, connected at pinout P3, with an associated control software provided by ADI is also used to control the

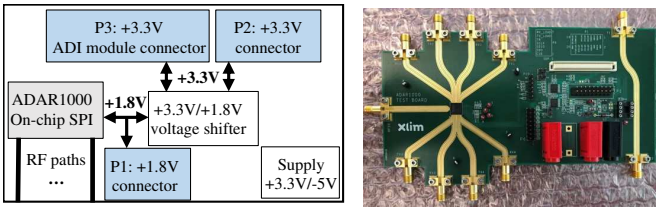
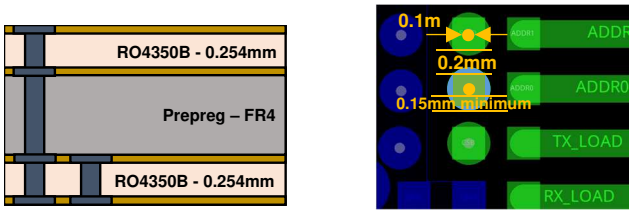


Fig. 2. Block diagram of the demonstration PCB (left) and the realized one for tests (right).

chip, giving more credibility to the measurement results. Supply voltages of 3.3 V and -5 V are required. A stackup with FR4-type prepreg and a 0.254 mm thick Rogers RO4350B substrate for RF microstrip lines, which will later be used and simulated in the antenna design, is realized (Fig.3a). The first RF layer serves as a feed layer from the chip's RF pins to the input/output measurement ports. The other layers provide ground planes, power planes and routing space. Thru vias with a minimum diameter of 0.1 mm are employed, corresponding to small distances between the chip's pins (0.2 mm), the constraint of minimum annular ring for vias (0.15 mm for vias with diameter of 0.1 mm), and the minimum distance between vias from the manufacturer (Fig.3b). The manufactured PCB is presented in Fig.2. A thru line (on the right side) replicating the RF paths from/to the chip is laid out to observe on-board RF losses and to de-embed the beamformer's performance.



(a) (b)

Fig. 3. (a) Demonstration PCB stackup (b) Pin Via Constraint.

B. *Measurement of the demonstration PCB*

The testbench for the demonstration PCB is shown in Fig.4. The measurement setup is realized as shown in red. A fixed input power of -30 dBm, far below compression points of both RX and TX, is employed at this stage to ensure the accuracy of 2-port SP measurements. The measurement is first executed using the control module from ADI to confirm a few working states of the chip. Subsequently, an automatization of measurement is made to collect SP data from all states of amplitude and phase of each channel with NI I2C/SPI USB-8452 Interface Device. The VNA applies measurement automatically and consecutively for each loaded amplitude-phase state. A maximum gain of 8 dB and 18.5 dB is obtained for RX and TX, respectively. The chip provides less than 0.4 dB RMS amplitude variation and maximum 3 deg RMS phase error over all phase states within all sets of amplitudes. More than 10 dB return loss is sustained in the frequency band of 8 GHz - 16 GHz. Maximum gains and reflection coefficients are given in Fig.5a. Relative phase shifts resulted from 0-deg to 360-deg settings with steps of 5.625 deg are shown in Fig.5b.

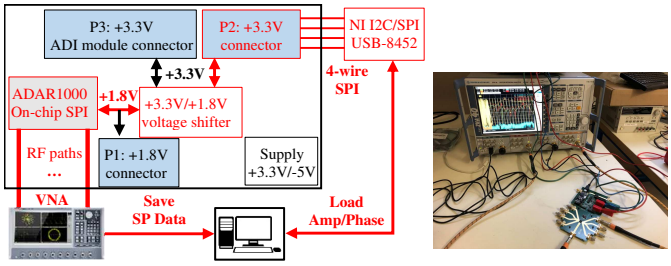


Fig. 4. Testbench of the demonstration PCB.

The RMS phase error and RMS amplitude variation results are provided in Fig.5c. The measured gains in Fig.5a are 3-4 dB lower than those reported in the datasheet of the ADAR1000 due to path losses. These losses are confirmed through the measurement of the thru line. The de-embedded gain results at the chip's pins of the proposed demonstration PCB are compared to the provided de-embedded gains from ADI's PCB in Fig.5d. A good agreement is observed.

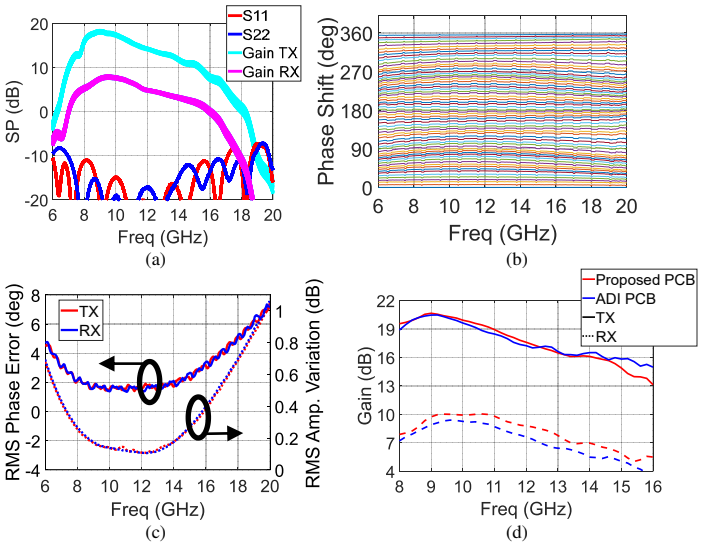


Fig. 5. Measured (a) $|S_{ii}|_{dB}$ and max. gains at all phase states (b) Relative Phase Shifts at max. gain (c) RMS Phase and Amp. Variation (d) De-embedded max. gains, comparison between our board and the ADI reference design.

Further comparisons are made between the measurement results of the proposed PCB and the original one in Fig.6. To maintain practicality, the rest of the results will be shown with path losses included. A fluctuation of ±6 deg in raw phase products of the same phase setting is observed between the 4 RX and TX. A comparison of different boards is also made to observe the variation in chip performance under soldering and part-to-part effects, in which a gain variation of 1 dB is noted between different chips and different PCBs. Results of 1-dB compression point (P1dB) are shown in Fig.7, obtained through Keysight PNA-X network analyzer's SMART Sweep process. Fig.7 also shows third-order intercept point (IP3) obtained by using a 2-tone signal with 1 MHz spacing and center frequency swept between 8 GHz and 16 GHz, at an input of -30 dBm. Lastly, amplitude(dB)-phase(deg) presentations of all measured states in polar coordinates are shown in Fig.8, indicating the range of produced gains and phase shifts from a single channel

of the RFIC. Table I summarizes the measurement results in comparison with measurement data from the evaluation board from ADI and data from the datasheet of the ADAR1000. The measurement results are consistent with the datasheet.

Table I. Characterization Results Summary.

Parameter		*Proposed PCB*	*ADI ref PCB*	*Datasheet ADAR1000*
Freq. Range (GHz)		8 - 16		
Amp. Adjust. Range (dB)		37 - 42		> 31
Total RF path length		$4.5\lambda_{max}$	$6\lambda_{max}$	--
Max Channel Gain (dB) at 9.5 GHz	TX	18.5	17	--
	RX	8.5	6.5	--
De-embedded max. gain (dB) at 9.5 GHz	TX	20	20	21
	RX	10	9	10
Output P1dB (dBm)	TX	9		10
Input P1dB (dBm)	RX	-14		-16
Output IP3 (dBm)	TX	19		20
Input IP3 (dBm)	RX	-5		-7
RMS Amp. Var. (dB)		< 0.4		0.2 typ.
RMS Phase Error (deg)		< 3		2 typ.
Amp. Flatness (dB)		±0.8		±1.7

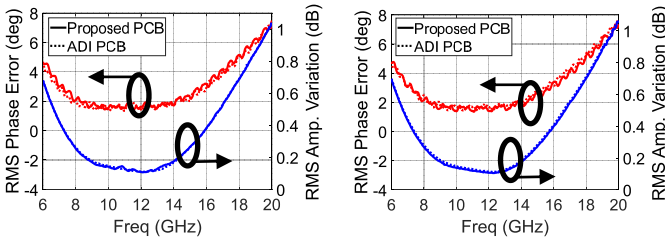


Fig. 6. RMS Errors comparisons (left) TX and (right) RX.

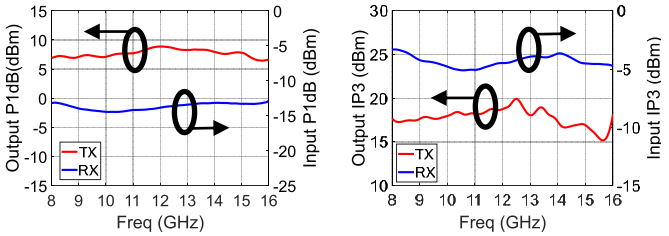


Fig. 7. (left) P1dB and (right) IP3 Measurement Results.

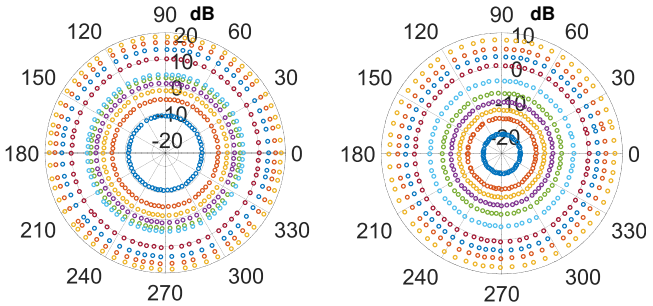
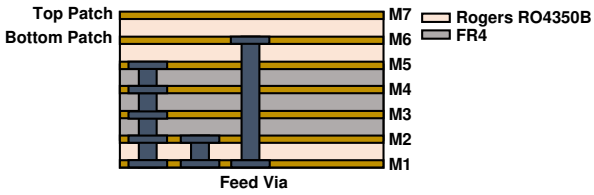


Fig. 8. Amplitude-Phase states at 9.5GHz of (left) TX and (right) RX.

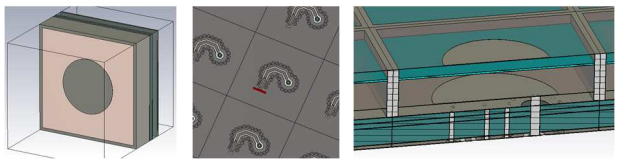
III. Design of the Radiating Panel in Ku Band

The antenna array to be integrated with the ADAR1000 Beamformer is designed in CST Studio Suite. The Unit Cell method is implemented for a square lattice, considering an element in an array with an infinite number of elements. The Floquet ports allow the calculation of fields radiated from a unit cell element at different scan elevation angles, under the coupling effects from other cells. The designed matching frequency band for the array is 11.7 GHz – 12.2 GHz (4% BW), which is the working band of many SATCOM low-noise block downconverters in Ku band for SATCOM TV broadcasting. An extended stackup of Rogers RO4350B and FR4 is implemented in the design owing to their close Coefficients of Thermal Expansion (CTE) in the x-, y-, and z-axis, making the stackup more feasible and sustainable (Fig.9a). The first 4 layers (M1 to M4) are kept unchanged to those from the demonstration board in Fig.3a. The intermediate substrate between M3 and M4 is changed to FR4 to facilitate manufacturing and reduce the risks from thermal expansion. The unit cell is presented in Fig.9b. A stacked-patches configuration (M6 and M7) is selected for its wide-bandwidth characteristics. A metallic grid surrounds the unit cell at the patches' levels to prevent surface waves from degrading matching performances. In this design, the feed begins at the chip's RF pin on M1, represented by a 50-Ohm waveguide port (Fig.9c), feeding the driven patch through a via (Fig.9d). The unit cell is optimized at scan angles up to 40 deg off-boresight in elevation. A matching band of 11.3 GHz – 12.8 GHz (12% BW) is achieved for various azimuth planes.

The active reflection coefficients at different directions {θ;φ} are given in Fig.10. In addition, the active element pattern (Fig.10) shows no scan blindness [5]. Furthermore, a 4x4 array (for 4 ADAR1000 chips) is simulated using the EM full-wave engine. The array will be used in the co-simulation with the measurement data from the ADAR1000 beamformer. The elements are simultaneously fed to obtain the performance of a finite array and achieve comparable results with those from the Unit Cell method, while considering edge effects. The matching bandwidth slightly decreases due to the finite array.



(a)



(b) (c) (d)

Fig. 9. (a) Antenna array stackup for RFIC integration - Unit Cell's (b) top view (c) bottom view and (d) cut view.

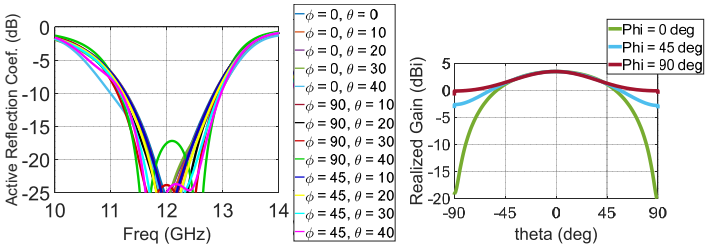


Fig. 10. (left) active reflection coefficients of the unit cell for elevation scan angles up to 40 deg off-boresight (right) active element realized gain pattern.

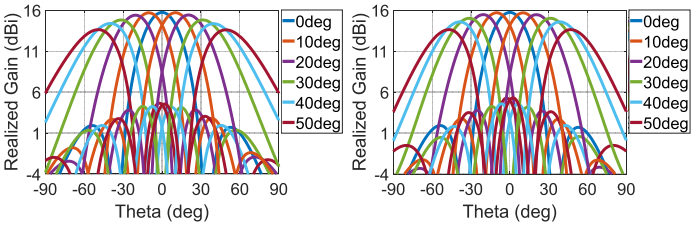


Fig. 11. Realized Gain Patterns at 12 GHz in (left) E-plane and (right) H-plane of the 4x4 array.

Nevertheless, the acquired bandwidth is sufficient for the intended applications in Ku band, and for the integration with four ADAR1000 beamformers. The realized gain patterns of the 4x4 array in E-plane and H-plane are given in Fig.11. A scan loss of around 3 dB at 50 deg scanning is shown, providing a practical $cos^{1.5}\theta$ scan loss curve for typical designs [6].

IV. Co-simulation of Characterization Data and Full-Wave Simulation Results of the Radiating Panel

The co-simulation between the RFIC characterization data and the 4x4 array is made to check the radiation patterns after considering amplifiers gains and phase shifts from the RFIC. The simulation is set in the CST Schematic. 16 simulation ports of the 4x4 array are cascaded to 16 Touchstone blocks, representing the connections between the RFIC inputs/outputs and the antenna ports.

An automatization process through VBA script is run to automatically select the measurement data corresponding to the required amplitude and phase settings at the simulated scan angle. The selected data is loaded to the Touchstone blocks, considering the progression of relative phase shifts between elements, i.e. beam-steering scenario. Each channel's phase shift and gain are hence from the RFIC measurement. Far-field results from the full-wave simulation of the 4x4 array are combined with the added gains and phase shifts from the touchstone blocks. Only results from maximum-amplitude settings for both RX and TX are shown in this paper.

Fig. 12 shows the combined results of the co-simulation. For both RX and TX, it is observed that the coherent gain at each scan angle is the sum of the gains from the 16 elements' channels added by the gains of the RFIC's channels at the corresponding phase shift progression setting. For instance, at 12 GHz in boresight, each RX channel and TX channel is added with 4.7 dB and 14.5 dB of gain from the RFIC in Fig.5a, respectively. Consequently, the coherent (combined) gains in boresight of the array increase by 4.7 dB and 14.5 dB at 12 GHz for RX and TX (Fig.12a,c), respectively. Similar results can be obtained with different excitation weightings, which indicates a correct integration and validates the array design.

Furthermore, it should be noted that at this stage, nonlinear effects are not considered. Complementary models of the RFIC are currently in progress, with the use of data from load-pull measurements of the RFIC, to enhance the accuracy of the co-simulation. To take these bilateral interactions into account, a system-level simulator from AMCAD Engineering, VISION [7], will be used with a dedicated gateway.

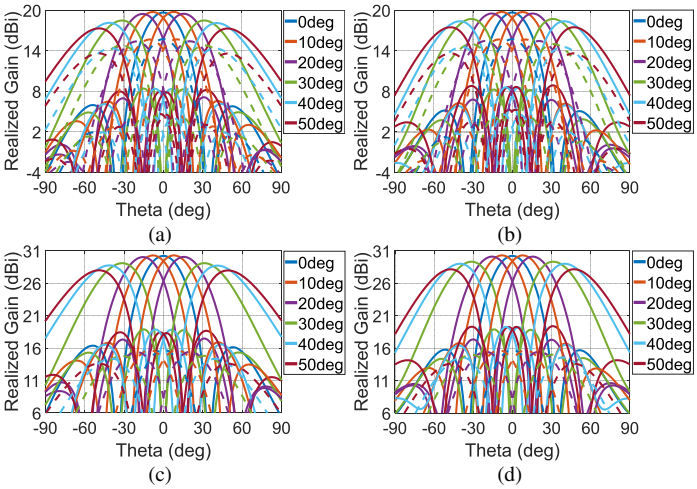


Fig. 12. Co-simulation Realized Gain Patterns at 12 GHz in (a) E-plane and (b) H-plane for RX and (c) E-plane and (d) H-plane for TX.
Continuous lines: combined results with measured RFIC gains/phase shifts
Dashed lines: full-wave simulation results with ideal phase shifts only (Fig.11).

V. Conclusion

A rigorous methodology in the workflow of RFIC-and-array integration is proposed. The characterization, design and integration co-simulation results confirm the validity of the process. Automatization procedures are included in the characterization and co-simulation to save time. The collected results are useful references for the measurement of the manufactured array. Such a guideline facilitates detecting defects in the integration stages and is applicable for all integration processes. It is also powerful for the optimization of excitation weightings and calibration.

Acknowledgment

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